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| EXAMINER | |
|---|---|
| TABONE JR, JOHN J | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2138 | |

DATE MAILED: 07/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/709,389 | GRUPP ET AL. | |
| | Examiner | Art Unit | |
| | John J. Tabone, Jr. | 2138 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *30 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04302006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-30 have been examined.

### *Information Disclosure Statement*

2. The information disclosure statement (IDS) submitted on 04/30/2004 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

### *Specification*

3. The disclosure is objected to because of the following informalities:

a. Entire disclosure is missing page numbers. Page numbers should be added in response to this office action.

b. A space needs to be added between IEEE and 1149.1. Starting at Paragraph 5 and throughout the specification "IEEE1149.1" needs to be changed to "IEEE 1149.1".

Appropriate correction is required.

4. Toward the end paragraph 29 with respect to the discussion of Fig. 4, "TAP string #1" should be "TAP string #2". Also, "TAPs 1a 1n 400-402" should be "TAPs #1a, 1b...1n, 400-402".

***Claim Objections***

The following is a quotation of 37 CFR § 1.75(i):

> (i.) Where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation.

5. **Claims 1-30 objected to** for containing a plurality of elements or steps, which are not separated by a line indent. An amendment is required to put the claim in proper format. Line indents aid in understanding the logical grouping of a claim's elements.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 3 recites the limitation "the active segments" in line 5. There is insufficient antecedent basis for this limitation in the claim.

7. Claim 7 recites the limitation "the active length" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

8. Claims 12 and 17 recite the limitation "the active length" in line 5. There is insufficient antecedent basis for this limitation in the claim.

9. Claims 19 and 26 recite the limitation "the active length" in line 2. There is insufficient antecedent basis for this limitation in the claim.

10. Claim 22 recites the limitation "the active length" in line 17. There is insufficient antecedent basis for this limitation in the claim.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. Claims 1-28 and 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Jacobson (US007073110), hereinafter Jacobson.

**Claim 1:**

Jacobson teaches a chip level test access port (TAP) controller having a chip-level TAP instruction register (**Host TAP 320, Fig. 3a**) and a plurality of embedded TAPs connected to said chip level TAP (**IP Core TAP 318, Fig. 3a**), said embedded TAPs having instruction register lengths that differ from said chip-level TAP instruction register, and wherein said chip level TAP includes a flexible length instruction register (**Programmable Instruction Register and Logic 304, Fig. 3a**) adapted to accommodate different length instruction registers of said embedded TAPs. (Col. 3, ll. 16-38, col. 7, ll. 21-64, col. 8, l. 49 to col. 9, l. 51).

**Claim 10:**

Jacobson teaches a chip level test access port (TAP) controller having a chip-level TAP instruction register (**Host TAP 320, Fig. 3a**) and a plurality of embedded TAPs connected to said chip level TAP (**IP Core TAP 318, Fig. 3a**), said embedded

TAPs having instruction register lengths that differ from said chip level TAP instruction register, and at least some of the embedded TAP instruction register lengths may differ from each other, wherein said chip level TAP includes a flexible length instruction register (**Programmable Instruction Register and Logic 304, Fig. 3a**) adapted to accommodate different length instruction registers of said embedded TAPs. Jacobson also teaches said flexible length instruction register comprises a first instruction register segment (**fixed length instruction register 382, Fig. 3c**) having the same length as the shortest embedded TAP instruction register and a second instruction register segment (**bit registers 376, 378, . . . 380, Fig. 3c**) having a length equal to the difference between said shortest embedded tap instruction register and a larger embedded TAP instruction register. (Col. 3, ll. 16-38, col. 7, ll. 21-64, col. 8, l. 49 to col. 9, l. 51).

**Claim 15:**

Jacobson teaches a chip level test access port (TAP) controller having a chip-level TAP instruction register (**Host TAP 320, Fig. 3a**) and a plurality of embedded TAPs connected to said chip level TAP (**IP Core TAP 318, Fig. 3a**), said embedded TAPs having instruction register lengths that differ from said chip level TAP instruction register, and at least some of the embedded TAP instruction register lengths may differ from each other, wherein said chip level TAP includes a flexible length instruction register (**Programmable Instruction Register and Logic 304, Fig. 3a**) adapted to accommodate different length instruction registers of said embedded TAPs. Jacobson also teaches said flexible length instruction register comprises a first instruction register

segment (**fixed length instruction register 382, Fig. 3c**) having the same length as the shortest embedded TAP instruction register and additional instruction registers segments (**bit registers 376, 378, . . . 380, Fig. 3c**) having incremental lengths equal to the difference between the previous shorter embedded tap instruction register and the next largest embedded TAP instruction register. (Col. 3, ll. 16-38, col. 7, ll. 21-64, col. 8, l. 49 to col. 9, l. 51).

**Claim 22:**

Jacobson teaches a chip level test access port (TAP) controller (**Host TAP 320, Fig. 3a**) and a plurality of embedded TAPs connected to said chip level TAP (**IP Core TAP 318, Fig. 3a**), said embedded TAPs having instruction register lengths that differ from said chip level TAP instruction register, and at least some of the embedded TAP instruction register lengths may differ from each other, wherein said chip level TAP includes a flexible length instruction register (**Programmable Instruction Register and Logic 304, Fig. 3a**) adapted to accommodate different length instruction registers of said embedded TAPs. Jacobson also teaches said flexible length instruction register is longer than the longest embedded TAP instruction register (**Programmable Instruction Register and Logic 304c, Fig. 3c**). Jacobson further teaches additional bits that make said flexible length instruction register longer than the longest embedded TAP instruction register comprises bits that are adapted to choose the active length of said flexible length instruction register (**bit registers 376, 378, . . . 380 coupled to a selector 370, 372, . . . 374 respectively, Fig. 3c**). (Col. 3, ll. 16-38, col. 7, ll. 21-64, col. 8, l. 49 to col. 9, l. 51).

Claim 2, 11 and 16:

Jacobson teaches said flexible length instruction register is longer than the longest embedded TAP instruction register (**Programmable Instruction Register and Logic 304c, Fig. 3c**). (Col. 8, l. 49 to col. 9, l. 51).

Claim 3, 12 and 17:

Jacobson teaches additional bits that make said flexible length instruction register longer than the longest embedded TAP instruction register comprises bits that are adapted to choose the active segments of said flexible length instruction register (**bit registers 376, 378, . . . 380 coupled to a selector 370, 372, . . . 374 respectively, Fig. 3c**). (Col. 8, l. 49 to col. 9, l. 51).

Claim 4 and 23:

Jacobson teaches said flexible length instruction register comprises a first instruction register segment (**fixed length instruction register 382, Fig. 3c**) having the same length as the shortest embedded TAP instruction register and a second instruction register segment (**bit registers 376, 378, . . . 380, Fig. 3c**) having a length equal to the difference between said shortest embedded tap instruction register and a larger embedded TAP instruction register. (Col. 3, ll. 16-38, col. 7, ll. 21-64, col. 8, l. 49 to col. 9, l. 51).

Claim 5 and 24:

Jacobson teaches said flexible length instruction register comprises a first instruction register segment (**fixed length instruction register 382, Fig. 3c**) having the same length as the shortest embedded TAP instruction register and additional

instruction registers segments (**bit registers 376, 378, . . . 380, Fig. 3c**) having incremental lengths equal to the difference between the previous shorter embedded tap instruction register and the next largest embedded TAP instruction register. (Col. 3, ll. 16-38, col. 7, ll. 21-64, col. 8, l. 49 to col. 9, l. 51).

Claim 6, 18 and 25:

Jacobson teaches a plurality of multiplexors connected to said additional instruction register segments (**selectors 370, 372, . . . 374, Fig. 3c**), wherein said multiplexors are adapted to selectively include incremental ones of said additional instruction register segments to incrementally match the difference in length between longer embedded TAP instruction registers and the chip-level TAP instruction register length. (Col. 8, l. 49 to col. 9, l. 51).

Claim 7, 19 and 26:

Jacobson teaches the active length of said flexible length instruction register comprises the selected ones of said additional instruction registers segments. (Col. 8, l. 49 to col. 9, l. 51).

Claim 8, 13, 20 and 27:

Jacobson teaches said flexible length instruction register appears as a fixed length instruction register to users connecting to said chip level TAP. (Col. 8, l. 49 to col. 9, l. 51).

Claim 9, 14, 21 and 28:

Jacobson teaches selection logic adapted to actively connect only a single embedded TAP at a time to said chip level TAP (**the IMUXes 316, 326 and OMUXes**

**316, 324 can connect to the IP processor core(s) and the JTAG TAP signals TCK 330, TDI 322, TDO 336, and TMS 332**). (Col. 7, ll. 21-40).

Claim 30:

Jacobson teaches the number of said embedded TAPs is unlimited in that the invention is not limited to the precise arrangements shown in FIG. 1. (Col. 7, ll. 38-40). Jacobson also teaches although only connections to the IP processor core IR 338 and IP processor core DR1 340 and IP processor core DR2 342 are shown, the invention is not limited in this regard. (Col. 7, ll. 44-47).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claim 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobson (US007073110), hereinafter Jacobson, in view of Nadeau-Dostie et al. (US-6829730), hereinafter Nadeau-Dostie.

Claim 29:

Jacobson does not explicitly disclose that the "**embedded TAPs comprise serially connected TAPs**". Nadeau-Dostie illustrates in an analogous art a Master TAP 100 and three embedded TAPS 102, 104 and 106, shown by dotted rectangles. Nadeau-Dostie teaches TAPs 104 and 106 are located in group 114 and have

instruction registers 118 and 120, respectively, each also having three shift register elements. Instruction registers 104 and 106 are serially connected in a serial or daisy chain (**embedded TAPs comprise serially connected TAPs**) between a group TDI node 122 and a group TDO node 124. Group 114 has the longest instruction register chain length of the embedded groups, having a total of six shift register elements or bits. (Fig. 3, Col. 9, l. 47 to col. 10, l. 17). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Jacobson's TAP configuration with Nadeau-Dostie TAP configuration in order to serially connect IP Core TAP(s) 318. The artisan would be motivated to do so because it would enable Jacobson to serially string different embedded core TAPs 318 in order to save test time.

## *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

John J. Tabone, Jr.
Examiner
Art Unit 2138

7/10/06

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